In the Claims:

1. (original) An integrated circuit comprising:

a body bias distribution circuit;

a pad coupled to said body bias distribution circuit, said pad for receiving an externally applied voltage;

an internal voltage bus; and

a circuit component coupled to said internal voltage bus and coupled to said body bias distribution circuit, wherein said internal voltage bus supplies a body bias voltage to said distribution circuit absent a voltage applied to said pad.

2. (original) An integrated circuit as described in Claim 1 wherein said externally applied voltage is substantially applied to said distribution circuit when said externally applied voltage is applied to said pad.

3. (original) An integrated circuit as described in Claim 2 wherein said circuit component is a resistor element.

4. (original) An integrated circuit as described in Claim 2 further comprising an external pin coupled to said pad, said external pin for coupling with said externally supplied voltage.

5. (original) An integrated circuit as described in Claim 2 wherein said internal voltage bus is coupled to a power supply voltage of said integrated circuit.

6. (original) An integrated circuit as described in Claim 1 further comprising a plurality of metal oxide semiconductor transistors coupled to said body bias distribution circuit.

7. (original) An integrated circuit as described in Claim 6 wherein said plurality of metal oxide semiconductor transistors are coupled to said distribution circuit via respective body terminals.

8 – 14 (canceled) (restriction)

15-21 (canceled)

22 – 34 (canceled) (restriction)

35. (original)A method of providing a body bias voltage in a semiconductor device comprising:

responsive to a coupling of an external body bias voltage to said semiconductor device, coupling said body bias voltage to body biasing wells of said semiconductor device; and

responsive to an absence of said external body bias voltage, automatically supplying said body biasing wells of said semiconductor device with an internal voltage of said semiconductor device through a resistance.

36. (original)The method of Claim 35 wherein said internal voltage is a power supply voltage for said semiconductor device.

37. (original)The method of Claim 35 wherein said internal voltage is a ground reference for said semiconductor device.

38. (original)The method of Claim 35 wherein said resistive structure comprises an n well region.

39. (original)The method of Claim 35 wherein said resistive structure forms a desired resistance between said internal voltage and said n well channels.

40. (original)The method of Claim 39 wherein said desired resistance is about 1 kilo ohm.

41. (original)The method of Claim 35 wherein said resistance is at least about one hundred times as large as a resistance of said coupling of said body bias voltage to said body biasing wells of said semiconductor device.